OpenCPI
Timestamper Scdcd Component Data Sheet

OpenCPI Release: v2.4.7

Revision History

Revision	Description of Change	Date
v2.0	Update doc and fix issues	08/2020

Summary - Timestamper Scdcd

Name	timestamper_scdcd
Worker Type	Application
OpenCPI Release	v2.4.7
Last Update	09/2020
Component Library	ocpi.assets.util_comps
Workers	timestamper_scdcd.hdl
Tested Platforms	xsim (Vivado 2017.1) zed

Summary - Timestamper Scdcd

Functionality

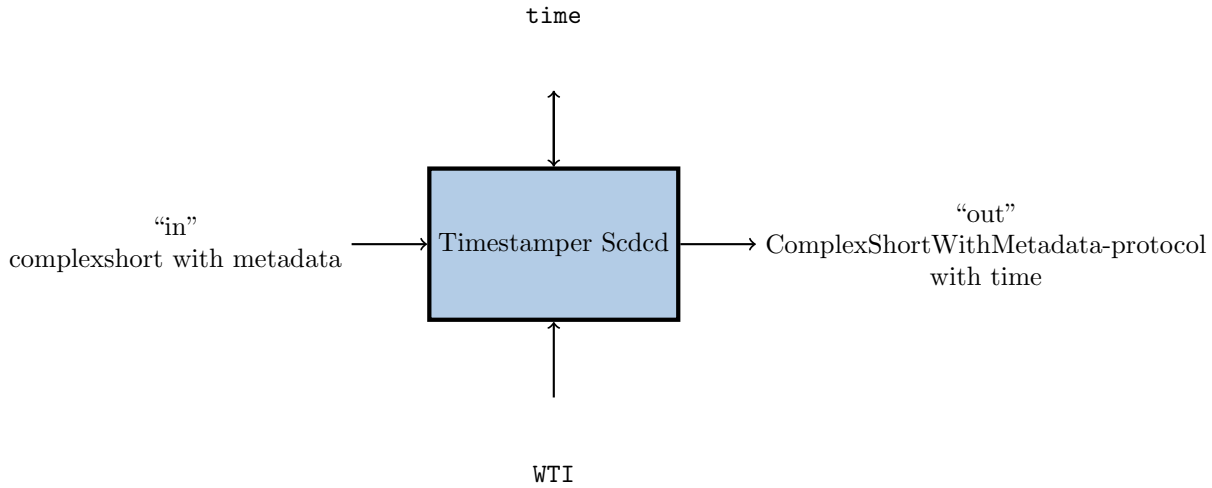
The timestamper_scdcd component contains the properties and ports for facilitating timestamping of complex samples with separate control and data clock domains (hence the name "scdcd"). Note that the actual separation of the clock domain is enforced by the HDL OWD, and not the OCS.

Worker Implementation Details

The timestamper_scdcd.hdl worker has separate clock domains for the `in` port, `out` port, and control plane. The `in` and `out` ports are supplied with separate clocks from their connected workers. Timestaping is done by sending ComplexShortWithMetadata-prot time opcode messages whose fract_sec and sec arguments contain the values provided by the fraction elements and seconds, respectively, of the `time` TimeInterface. The `time` TimeInterface is supplied with the `in` port's clock. Input messages with the time opcode are not passed through. Messages received on the input port with samples and sync opcodes, along with the formed time messages, cross from the `in` clock domain to the `out` clock domain via an asynchronous FIFO, and are sent to the `out` port.
IMPORTANT: As a reminder, the input messages with the time opcode are not passed through.

Block Diagrams

Top level



Source Dependencies

timestamper_scdcd.hdl

- projects/assets/components/util_comps/timestamper_scdcd.hdl/timestamper_scdcd.vhd
- projects/assets/components/util_comps/timestamper_scdcd.hdl/cdc_fifo_complex_short_with_metadata.vhd
- projects/assets/hdl/primitives/misc_prims/misc_prims_pkg.vhd
- projects/assets/hdl/primitives/misc_prims/misc_prims_body.vhd
- projects/assets/hdl/primitives/misc_prims/level_to_pulse_converter.vhd
- projects/core/hdl/primitives/cdc/cdc_pkg.vhd
- projects/core/hdl/primitives/cdc/fifo.vhd
- projects/core/hdl/primitives/cdc/fast_pulse_to_slow_sticky.vhd
- projects/core/hdl/primitives/cdc/single_bit.vhd
- projects/assets/components/misc_comps/cswm_to_iqstream.hdl/cswm_to_iqstream.vhd
- projects/assets/components/misc_comps/iqstream_to_cswm.hdl/iqstream_to_cswm.vhd
- projects/core/hdl/primitives/util/util_pkg.vhd
- projects/core/hdl/primitives/util/util_body.vhd
- projects/core/hdl/primitives/ocpi/zlm_detector.vhd
- projects/assets/hdl/primitives/misc_prims/time_downsampler.vhd
- projects/assets/hdl/primitives/misc_prims/advance_counter.vhd
- projects/assets/hdl/primitives/misc_prims/cdc_pkg.vhd
- projects/assets/hdl/primitives/misc_prims/cdc_fifo_info.vhd
- projects/core/hdl/primitives/util/set_clr.vhd
- projects/core/hdl/primitives/protocol/message_sizer.vhd

Component Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Description
bypass	Bool	-	-	Writable	Standard	False	Forces in port messages to be sent directly to out port, bypassing the timestamping functionality.
time_correction	Longlong	-	-	Writable	Standard	0	Q32.32 time correction value which is subtracted from the applied time (note Qm.n implies existence of a sign bit).
correction_overflow_sticky	Bool	-	-	Volatile	Standard	-	Sticky bit overflow indication of correction calculation.
clr_correction_overflow_sticky	Bool	-	-	Writable	Standard	False	Writing a value of true clears correction_overflow_sticky.
force_error_on_invalid_time_at_start	Bool	-	-	Initial	Standard	False	Forces worker into the unusable state if the time invalid signal is low during the worker initialized state.
samples_per_timestamp	Ulong	-	-	Writable	Standard	1m	After each timestamp, this number of samples is passed before the next one. If zero, a timestamp precedes each sample output message (not recommended).
sampling_interval	Ulonglong	-	-	Writable	Standard	0	The fraction of a second between samples, in Q0.64 fixed point format. Send in the stream if non-zero, upon start or when written

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timestamper_scdcd.hdl

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IN_PORT_DATA_WIDTH	Uchar	-	-	Parameter	Standard	32	-

OUT_PORT_DATA_WIDTH	Uchar	-	-	Parameter	Standard	32	-
CTRL_IN_CDC_DEPTH	Ushort	-	-	Parameter	Standard	16	-
DATA_CDC_DEPTH	Ushort	-	-	Parameter	Standard	16	-

Component Ports

Name	Producer	Protocol	Optional
in	False	ComplexShortWithMetadata-prot	False
out	True	ComplexShortWithMetadata-prot	False

Worker Interfaces

timestamper_scdcd.hdl

Type	Name	Producer	Protocol	Optional	DataWidth	Clock	ClockDirection	WorkerEOF	InsertEOM
StreamInterface	in	False	ComplexShortWithMetadata-prot	False	IN_PORT_DATA_WIDTH	-	in	False	False
StreamInterface	out	True	ComplexShortWithMetadata-prot	False	OUT_PORT_DATA_WIDTH	-	in	True	True

Control Timing and Signals

The timestamper_scdcd worker uses three sepearte clocks. The input and output ports use clocks that are seperate from the clocks of the workers they are connected to. The timestamper_scdcd worker also uses a clock from the Control Plane for the previously mentioned worker and the WCI. The timestamper_scdcd worker uses standard control plane signals.

Worker Configuration Parameters

timestamper_scdcd.hdl

Performance and Resource Utilization

timestamper_scdcd.hdl

Test and Verification

The test for the timestamper_scdcd uses a ramp of 512 samples that is generated by the generate.py script. Multiple files are created with varying paramters. The first parameter,time correction, which can be -1,0, or 1. The second, mininum number of samples for each timestamp, can be 0,1,1024,4091,4092, or 4093. The last variable is forcing an error if there is an invalid time, which can be set to true or false.
For verification, the output file is checked to see if SAMPLES, SYNC and TIME messages were recieved. All possible opcodes are sent through the UUT, and then it is verified that the previously mentioned ones were recieved and pass. The test fails if there are 0 TIME/SAMPLES recieved and if any number other than 1 SYNC message is recieved. The output file is also compared to a positive ramp function for I values, and a negative ramp function for Q values.