OpenCPI
CSTS To IQstream Component Data Sheet

OpenCPI Release: v2.4.7

Revision History

Revision	Description of Change	Date
v2.2	Initial release	04/2021

Summary - CSTS To IQstream

Name	csts_to_iqstream
Worker Type	Application
OpenCPI Release	v2.4.7
Last Update	04/2021
Component Library	ocpi.assets.misc_comps
Workers	csts_to_iqstream.hdl
Tested Platforms	CentOS7, xsim, Zed

Summary - CSTS To IQstream

Functionality

This component receives `ComplexShortTimedSample` protocol messages from the `in` port and converts them to `iqstream` protocol messages that are transmitted to the `out` port. The messages for all possible `ComplexShortTimedSample` opcodes are ingested, but only those with the `sample` opcode are converted and sent out the `out` port. This is due to the fact that `ComplexShortTimedSample` has not only a data-related opcode, but multiple non-data-related opcodes, and the `iqstream` protocol only has a single, data-related opcode. All `out` port messages use the `iqstream` protocol's `iq` opcode.

Source Dependencies

csts_to_iqstream.hdl

- core/hdl/primitives/util/reset_detector.vhd
- core/hdl/primitives/protocol/iqstream_body.vhd
- core/hdl/primitives/protocol/iqstream_pkg.vhd
- core/hdl/primitives/protocol/message_sizer.vhd
- core/hdl/primitives/timed_sample_prot/complex_short_timed_sample_body.vhd
- core/hdl/primitives/timed_sample_prot/complex_short_timed_sample_package.vhd
- core/hdl/primitives/timed_sample_prot/complex_short_timed_sample_demarshaller.vhd
- core/hdl/primitives/protocol/iqstream_marshaller.vhd
- assets/components/misc_comps/csts_to_iqstream.hdl/csts_to_iqstream.vhd

Component Properties

The component has no properties.

Worker Properties

csts_to_iqstream.hdl

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Description
IN_PORT_DATA_WIDTH	Uchar	-	-	Parameter	Standard	32	-
OUT_PORT_DATA_WIDTH	Uchar	-	-	Parameter	Standard	32	-

Component Ports

Name	Producer	Protocol	Optional
in	False	complex_short_timed_sample-prot	False
out	True	iqstream_protocol	False

Worker Interfaces

csts_to_iqstream.hdl

Type	Name	Producer	Protocol	Optional	DataWidth	Clock	ClockDirection	WorkerEOF	InsertEOM
StreamInterface	in	False	complex_ short_ timed_ sample- prot	False	IN_PORT_ DATA_WIDTH	-	in	False	False
StreamInterface	out	True	iqstream_ protocol	False	OUT_PORT_ DATA_WIDTH	in	-	True	False

Test and Verification

The Unit Under Test (UUT) is tested by a) generating a file containing protocol-formatted messages which are sent to the UUT via the `file_read` component, b) using the `file_write` component to save the file containing the UUT's output as protocol-formatted message, and c) verifying the contents of the output file. The generated file contains one or more `ComplexShortTimedSample samples` messages following followed by a message for each of the non-`sample` opcodes. The sequence of `samples` messages include samples whose I (Real) and Q (imaginary) signals are positive and negative ramp functions, respectively. The output file is verified by confirming that a) the same number of samples exists in the input and output files, and b) the output file contains the same ramp functions as the input.

Block Diagram