

OpenCPI  
AD9361 Data Sub Component Data Sheet

OpenCPI Release: v2.4.7

## Summary - AD9361 Data Sub

|                   |                                                                                                                                                                                                                                                                                              |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name              | ad9361_data_sub                                                                                                                                                                                                                                                                              |
| Worker Type       | Device                                                                                                                                                                                                                                                                                       |
| OpenCPI Release   | v2.4.7                                                                                                                                                                                                                                                                                       |
| Last Update       | 10/2018                                                                                                                                                                                                                                                                                      |
| Component Library | ocpi.assets.devices                                                                                                                                                                                                                                                                          |
| Workers           | ad9361_data_sub.hdl                                                                                                                                                                                                                                                                          |
| Tested Platforms  | <ul style="list-style-type: none"> <li>• Agilent Zedboard/Analog Devices FMCOMMS2</li> <li>• Agilent Zedboard/Analog Devices FMCOMMS3</li> <li>• x86/Xilinx ML605/Analog Devices FMCOMMS2</li> <li>• x86/Xilinx ML605/Analog Devices FMCOMMS3</li> <li>• Ettus E310 (Vivado only)</li> </ul> |

## Functionality

The AD9361 Data Sub is a subdevice worker that interfaces with the AD9361 IC[1]'s DATA\_CLK\_P/DATA\_CLK\_N, P0\_D[11:0], P1\_D[11:0], RX\_FRAME\_P, RX\_FRAME\_N, TX\_FRAME\_P, TX\_FRAME\_N, TXNRX, and ENABLE pins. P0\_D and P1\_D pins are routed to whichever ad9361\_adc\_sub.hdl or ad9361\_dac\_sub.hdl device worker is appropriate for the given AD9361 data pin interface configuration.

## Worker Implementation Details

### ad9361\_data\_sub.hdl

This worker's LVDS\_p, HALF\_DUPLEX\_p, SINGLE\_PORT\_p, and SWAP\_PORTS\_p parameter properties enforce build-time configuration<sup>1</sup> for all of the possible AD9361 data pin interface configurations[2]:

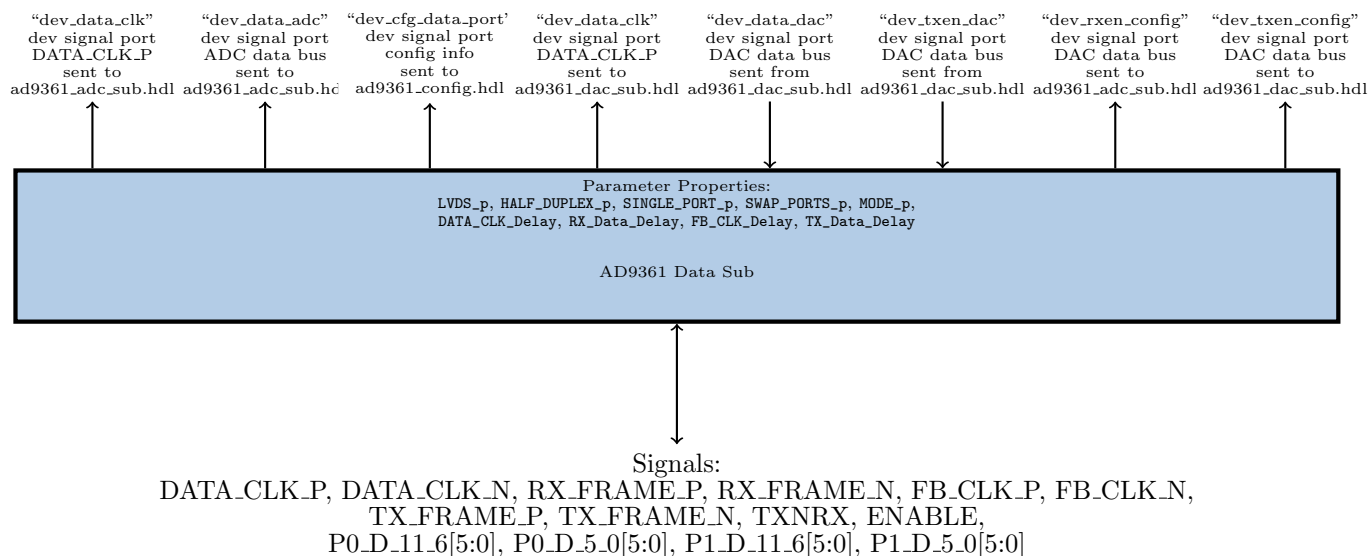
- CMOS Single Port Half Duplex,
- CMOS Single Port Half Duplex Swapped Ports,
- CMOS Single Port Full Duplex,
- CMOS Single Port Full Duplex Swapped Ports,
- CMOS Dual Port Half Duplex,
- CMOS Dual Port Half Duplex Swapped Ports,
- CMOS Dual Port Full Duplex,
- CMOS Dual Port Full Duplex Swapped Ports, and
- LVDS (Dual Port Full Duplex).

Note that the half duplex data interface formats allow for AD9361 P0/P1 port routing to be runtime-dynamic.

<sup>1</sup>Although this worker successfully builds for all data interface configurations, LVDS is the only configuration which has been tested and fully verified.

## Block Diagrams

### Top level



## Source Dependencies

### ad9361\_data\_sub.hdl

- `assets/hdl/devices/ad9361_data_sub.hdl/ad9361_data_sub.cpp_vhd`

### Component Spec Attributes

| Attribute | Value |
|-----------|-------|
| NoControl | True  |

### Component Spec Properties

| Name | Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|------|------|----------------|-----------------|---------------|-------------|---------|-------|
| -    | -    | -              | -               | -             | -           | -       | -     |

### Worker Properties

ad9361\_data\_sub.hdl

| Scope    | Name          | Type   | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default                                                                                                                                                               | Usage                                                                                                               |
|----------|---------------|--------|----------------|-----------------|---------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| Property | LVDS_p        | Bool   | -              | -               | Parameter     | Standard    | False                                                                                                                                                                 | Use LVDS mode for Data/clock/frame signals, otherwise use CMOS mode. Default is CMOS/single-ended mode.             |
| Property | HALF_DUPLEX_p | Bool   | -              | -               | Parameter     | Standard    | False                                                                                                                                                                 | Use half duplex mode, otherwise use full duplex mode. Must be false when using LVDS mode.                           |
| Property | SINGLE_PORT_p | Bool   | -              | -               | Parameter     | Standard    | False                                                                                                                                                                 | Use single port, otherwise use both (dual) ports. Default is to use both ports. Must be false when using LVDS mode. |
| Property | SWAP_PORTS_p  | Bool   | -              | -               | Parameter     | Standard    | False                                                                                                                                                                 | Swaps Port 0 and Port 1. Must be false when using LVDS mode.                                                        |
| Property | MODE_p        | UShort | -              | -               | Parameter     | Standard    | lvds_p ? 7 :<br>single_port_p ?<br>(half_duplex_p<br>? (swap_ports_p<br>? 1 : 0) :<br>(swap_ports_p<br>? 3 : 2)) :<br>half_duplex_p ? 4<br>: swap_ports_p ? 6<br>: 5) | a convenience parameter to map the various options into 8 modes.                                                    |

|          |                |        |   |   |           |          |   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------|----------------|--------|---|---|-----------|----------|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Property | DATA_CLK_Delay | UShort | - | - | Parameter | Standard | - | Ushort representation of AD9361 SPI Register 0x006 - DATA_CLK Delay bits. These bits affect the DATA_CLK delay. The typical delay is approximately 0.3 ns/LSB. Minimum delay setting is 0x0 and maximum delay setting is 0xF. Set this value so that the data from the AD9361 meets FPGA setup/hold specifications. Because the DATA_CLK delay is specific to a platform or platform/-card, the value of this parameter property should be enforced wherever 1) a platform which instantiates this device worker is defined or 2) a platform with a card which instantiates this device worker is defined. There may be future framework features added to better facilitate such enforcement, but currently the only places where this enforcement is possible is in 1) a platform XML for a platform which instantiates this device worker, 2) a platform configuration for a card which includes this device worker, or 3) a container for a card which includes this device worker. |
| Property | RX_Data_Delay  | UShort | - | - | Parameter | Standard | - | Ushort representation of AD9361 SPI Register 0x006 - RX Data Delay bits. These bits affect the Rx data delay. The typical delay is approximately 0.3 ns/LSB. Minimum delay setting is 0x0 and maximum delay setting is 0xF. Set this value so that the data from the AD9361 meets FPGA setup/hold specifications. Because the Rx data delay is specific to a platform or platform/card, the value of this parameter property should be enforced wherever 1) a platform which instantiates this device worker is defined or 2) a platform with a card which instantiates this device worker is defined. There may be future framework features added to better facilitate such enforcement, but currently the only places where this enforcement is possible is in 1) a platform XML for a platform which instantiates this device worker, 2) a platform configuration for a card which includes this device worker, or 3) a container for a card which includes this device worker.     |

|          |               |        |   |   |           |          |   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|---------------|--------|---|---|-----------|----------|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Property | FB_CLK_Delay  | UShort | - | - | Parameter | Standard | - | Ushort representation of AD9361 SPI Register 0x007 - FB.CLK Delay bits. These bits function the same as DATA.CLK and RX data delays but affect the FB.CLK delay. Set this value so that the data from the AD9361 meets FPGA setup/hold specifications. Because the FB.CLK delay is specific to a platform or platform/card, the value of this parameter property should be enforced wherever 1) a platform which instantiates this device worker is defined or 2) a platform with a card which instantiates this device worker is defined. There may be future framework features added to better facilitate such enforcement, but currently the only places where this enforcement is possible is in 1) a platform XML for a platform which instantiates this device worker, 2) a platform configuration for a card which includes this device worker, or 3) a container for a card which includes this device worker.                                                                                          |
| Property | TX_Data_Delay | UShort | - | - | Parameter | Standard | - | Ushort representation of AD9361 SPI Register 0x007 - TX Data Delay bits. These bits function the same as DATA.CLK and RX data delays but affect the Tx.FRAME and TX Data delay. Tx frame sync is delayed the same amount as the data port bits. Set this value so that the data from the AD9361 meets FPGA setup/hold specifications. Because the Tx.FRAME/TX Data delay is specific to a platform or platform/card, the value of this parameter property should be enforced wherever 1) a platform which instantiates this device worker is defined or 2) a platform with a card which instantiates this device worker is defined. There may be future framework features added to better facilitate such enforcement, but currently the only places where this enforcement is possible is in 1) a platform XML for a platform which instantiates this device worker, 2) a platform configuration for a card which includes this device worker, or 3) a container for a card which includes this device worker. |

Component Ports

| Name | Producer | Protocol | Optional | Advanced | Usage |
|------|----------|----------|----------|----------|-------|
| -    | -        | -        | -        | -        | -     |

## Worker Interfaces

### ad9361\_data\_sub.hdl

| Type      | Name              | Count | Optional | Master | Signal             | Direction | Width | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----------|-------------------|-------|----------|--------|--------------------|-----------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DevSignal | dev_cfg_data_port | 1     | False    | False  | iostandard_is_lvds | Input     | 1     | Value is 1 if the buildtime configuration was for the LVDS mode and 0 otherwise.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|           |                   |       |          |        | p0_p1_are_swapped  | Input     | 1     | Value is 1 if the buildtime configuration was with the AD9361 P0 and P1 data port roles inverted and 0 otherwise.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| DevSignal | dev_data_clk      | 3     | True     | False  | DATA_CLK_P         | Input     | 1     | Buffered version of AD9361 DATA_CLK_P pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| DevSignal | dev_data_adc      | 1     | True     | False  | data               | Input     | 24    | Data bus driven by configuration-specific AD9361 pins corresponding to the RX data path:<br>* CMOS single port half duplex: [12'b0 P0_D[11:0]],<br>* CMOS single port full duplex: [18'b0 P0_D[5:0]],<br>* CMOS dual port half duplex: [P0_D[11:0] P1_D[11:0]],<br>* CMOS dual port full duplex: [12'b0 P0_D[11:0]],<br>* LVDS: [18'b0 RX_D[5:0]],<br>or, if ports are swapped:<br>* CMOS single port half duplex: [12'b0 P1_D[11:0]],<br>* CMOS single port full duplex: [18'b0 P1_D[5:0]],<br>* CMOS dual port half duplex: [P1_D[11:0] P0_D[11:0]],<br>* CMOS dual port full duplex: [12'b0 P1_D[11:0]],<br>* LVDS: (unsupported with port swap).      |
|           |                   |       |          |        | rx_frame           | Input     | 1     | Output of buffer whose input is the AD9361 RX_FRAME_P pin's signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| DevSignal | dev_data_dac      | 1     | True     | False  | data               | Output    | 24    | Data bus which drives configuration-specific AD9361 pins corresponding to the TX data path:<br>* CMOS single port half duplex: [12'b0 P0_D[11:0]],<br>* CMOS single port full duplex: [18'b0 P0_D[11:6]],<br>* CMOS dual port half duplex: [P0_D[11:0] P1_D[11:0]],<br>* CMOS dual port full duplex: [12'b0 P1_D[11:0]],<br>* LVDS: [18'b0 TX_D[5:0]],<br>or, if ports are swapped:<br>* CMOS single port half duplex: [12'b0 P1_D[11:0]],<br>* CMOS single port full duplex: [18'b0 P1_D[11:6]],<br>* CMOS dual port half duplex: [P1_D[11:0] P0_D[11:0]],<br>* CMOS dual port full duplex: [12'b0 P0_D[11:0]],<br>* LVDS: (unsupported with port swap). |
|           |                   |       |          |        | tx_frame           | Output    | 1     | Signal which will drive the output buffer which drives the AD9361 TX_FRAME_P pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| DevSignal | dev_txen_dac      | 1     | True     | False  | txen               | Output    | 1     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| DevSignal | dev_rxen_config   | 1     | True     | False  | rxen               | Input     | 1     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| DevSignal | dev_txen_config   | 1     | True     | False  | txen               | Input     | 1     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

## Subdevice Connections

| Supports Worker | Supports Worker Port | ad9361_data_sub.hdl Port | ad9361_data_sub.hdl Port Index |
|-----------------|----------------------|--------------------------|--------------------------------|
| ad9361_config   | dev_cfg_data_port    | dev_cfg_data_port        | 0                              |
|                 | dev_rxen_data_sub    | dev_rxen_config          | 0                              |
|                 | dev_txen_data_sub    | dev_txen_config          | 0                              |
|                 | dev_data_clk         | dev_data_adc             | 2                              |
| ad9361_adc_sub  | dev_data_clk         | dev_data_clk             | 0                              |
|                 | dev_data_from_pins   | dev_data_adc             | 0                              |
| ad9361_dac_sub  | dev_data_clk         | dev_data_clk             | 1                              |
|                 | dev_data_to_pins     | dev_data_adc             | 0                              |

## Control Timing and Signals

Because this worker does not include a control plane and serves purely as an IC pin buffering and routing mechanism, there are no latency or clock domain considerations. For considerations specific to the RX/TX data paths, see the supports-connected device worker data sheets for `ad9361_adc_sub.hdl`[3] and `ad9361_dac_sub.hdl`[4].

## Performance and Resource Utilization

### Worker Configuration Parameters

`ad9361_data_sub.hdl`

`ad9361_data_sub.hdl`

Because every possible parameter property combination of this worker has no control plane and no registered data paths, no registers or LUTS are used and the Fmax measurement does not exist.

## Test and Verification

The test outlined in [4] includes validation of this worker's functionality (for LVDS mode and CMOS Single Port Full Duplex DDR mode).

## References

- [1] AD9361 Datasheet and Product Info  
<http://www.analog.com/en/products/rf-microwave/integrated-transceivers-transmitters-receivers/wideband>
- [2] AD9361 Reference Manual UG-570  
[AD9361\\_Reference\\_Manual\\_UG-570.pdf](#)
- [3] AD9361 ADC Component Data Sheet  
[http://opencpi.gitlab.io/releases/v2.4.7/docs/assets/AD9361\\_ADC.pdf](http://opencpi.gitlab.io/releases/v2.4.7/docs/assets/AD9361_ADC.pdf)
- [4] AD9361 DAC Component Data Sheet  
[http://opencpi.gitlab.io/releases/v2.4.7/docs/assets/AD9361\\_DAC.pdf](http://opencpi.gitlab.io/releases/v2.4.7/docs/assets/AD9361_DAC.pdf)