

# OpenCPI

## SI5351 Component Data Sheet

OpenCPI Release: v2.3.4

## Summary - SI5351

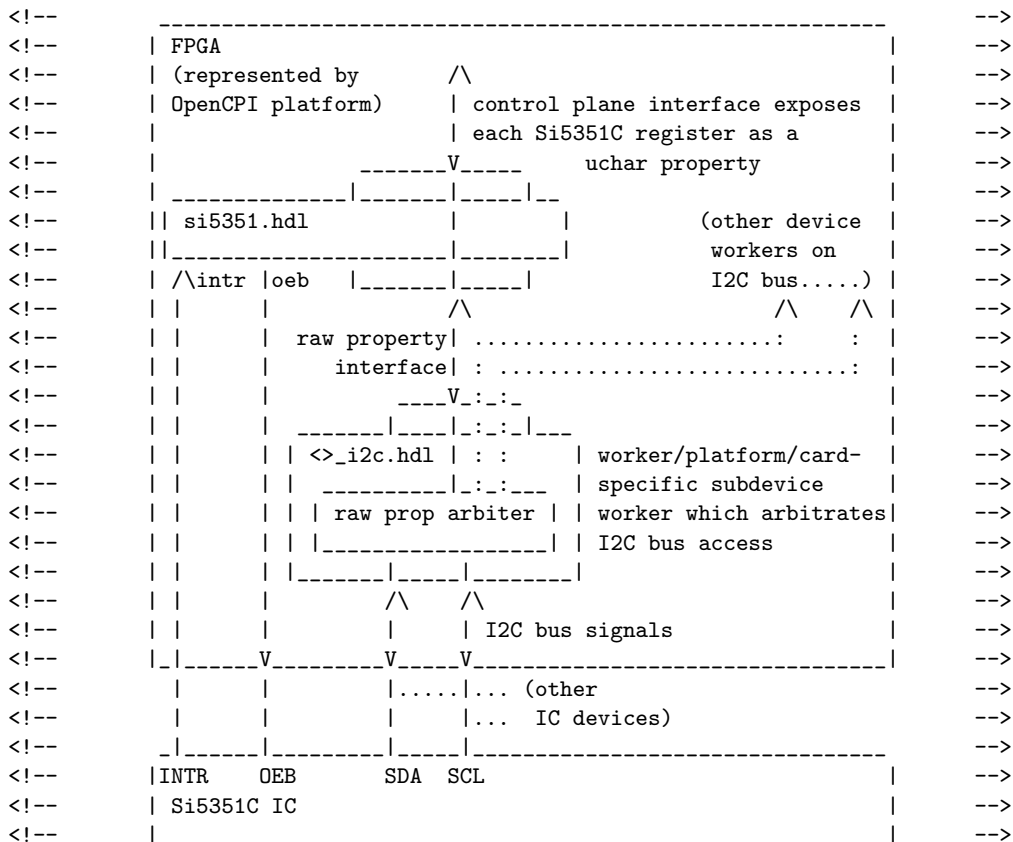
|                   |                                                 |
|-------------------|-------------------------------------------------|
| Name              | si5351                                          |
| Worker Type       | Device                                          |
| OpenCPI Release   | v2.3.4                                          |
| Last Update       | 4/2019                                          |
| Component Library | ocpi.assets.devices                             |
| Workers           | si5351.hdl                                      |
| Tested Platforms  | ALST4/Zipper, ML605/Zipper, ZedBoard(PL)/Zipper |

## Functionality

The SI5351 device worker exposes the register set of the Si5351C I<sup>2</sup>C clock generator IC[1] and directly interfaces with the IC's INTR and EOB pins. Each register is exposed as a uchar (8-bits wide) property. The worker drives the EOB pin to ground and the INTR pin's signal is currently unused. The Si5351C SDA/SCL pins are not controlled directly by this worker, but instead by a subdevice of this worker which arbitrates I2C bus access.

## Block Diagrams

### Top level



## Worker Implementation Details

### si5351.hdl - Property Set

Information about the static Si5351C hardware configuration is conveyed via the `clkin_present`, `clkin_freq`, `xtal_present`, `xtal_freq`, `vc_present`, `outputs_present`, `oeb_mode`, and `intr_connected` properties. Because these properties are designed to convey static information that is determined at build-time, their parameter attribute is set to true. Each of these properties also has its readable attribute set to true. Normally it is not recommended to set both the parameter and the readable attributes to true because readable implies unnecessary control plane infrastructure for property read accesses. Setting the parameter attribute alone to true exposes an optimized property read access mechanism for applications. This mechanism is not currently implemented, however, for device proxy slave interfaces. Because the aforementioned parameter properties are intended to be accessed via a device proxy slave interface, their readable attributes are set to true.

Each non-parameter property's value represents that of a Si5351C register. Each non-parameter property is a raw property.

### si5351.hdl - Control Plane Timeout Value Selection

Because I<sup>2</sup>C transactions require additional clock cycles to complete property accesses, the control plane timeout default value (of 16) is overridden to be 131072. The intended I<sup>2</sup>C SCL clock frequency is 250 kHz, and the I<sup>2</sup>C read operation duration is approximated to be 32 SCL clock cycles. This results in a read access being approximately  $32/(250,000 \text{ Hz}) = 0.000128 \text{ sec}$ . This corresponds to  $(\text{control plane clock cycles/sec}) * (0.000128 \text{ sec})$  clock cycles per read access. By setting the timeout to 131072, control plane clocks of up to approximately  $131072/0.00128 \text{ Hz} = 1.024 \text{ GHz}$  would be supported, which is far higher than any currently possible control plane clock frequency.

## Source Dependencies

### si5351.hdl

- `assets/hdl/devices/si5351.hdl/si5351.vhd`

## Component Spec Properties

| Name | Type | SequenceLength | ArrayDimensions | Accessibility | Valid Range | Default | Usage |
|------|------|----------------|-----------------|---------------|-------------|---------|-------|
| -    | -    | -              | -               | -             | -           | -       | -     |

## Worker Properties

### si5351.hdl

| Scope    | Name            | Type  | ArrayDimensions | Accessibility          | Padding | Valid Range        | Default | Usage                                                                                                                         |
|----------|-----------------|-------|-----------------|------------------------|---------|--------------------|---------|-------------------------------------------------------------------------------------------------------------------------------|
| Property | clk_in_present  | Bool  |                 | Parameter,<br>Readable |         |                    | 0       | Does this chip have an external clock as input?                                                                               |
| Property | clk_in_freq     | Float |                 | Parameter,<br>Readable |         |                    | 0       |                                                                                                                               |
| Property | xtal_present    | Bool  |                 | Parameter,<br>Readable |         |                    | 0       | Does this chip have a crystal oscillator as input?                                                                            |
| Property | xtal_freq       | Float |                 | Parameter,<br>Readable |         |                    | 0       |                                                                                                                               |
| Property | vc_present      | Bool  |                 | Parameter,<br>Readable |         |                    | 0       | Does this chip have a VCXO as input?                                                                                          |
| Property | outputs_present | Bool  | 8               | Parameter,<br>Readable |         |                    | 0       |                                                                                                                               |
| Property | oeb_mode        | Enum  |                 | Parameter,<br>Readable |         | low,high,connected | low     |                                                                                                                               |
| Property | intr_connected  | Bool  |                 | Parameter,<br>Readable |         |                    | 0       |                                                                                                                               |
| Property | dev_status      | UChar |                 | Readable               |         |                    |         | Hardware registers: 0: Device Status                                                                                          |
| Property | int_sts_stcky   | UChar |                 | Volatile,<br>Writable  |         |                    |         | Hardware registers: 1: Interrupt Status Sticky                                                                                |
| Property | int_sts_mask    | UChar |                 | Readable,<br>Writable  |         |                    |         | Hardware registers: 2: Interrupt Status Mask                                                                                  |
| Property | out_en_ctl      | UChar |                 | Readable,<br>Writable  |         |                    |         | Hardware registers: 3: Output enable control                                                                                  |
| Property | reserved00      | UChar | 5               |                        | true    |                    |         | Hardware registers: 4-8: Reserved                                                                                             |
| Property | oeb_pin_en      | UChar |                 | Volatile,<br>Writable  |         |                    |         | Hardware registers: 9: OEB pin enable control mask                                                                            |
| Property | reserved01      | UChar | 5               |                        | true    |                    |         | Hardware registers: 10-14: Reserved                                                                                           |
| Property | pll_in_src      | UChar |                 | Readable,<br>Writable  |         |                    |         | Hardware registers: 15: PLL Input Source                                                                                      |
| Property | clk_ctl         | UChar | 8               | Readable,<br>Writable  |         |                    |         | Hardware registers: 16 - 23: Clock Control                                                                                    |
| Property | clk30_dis_st    | UChar |                 | Volatile,<br>Writable  |         |                    |         | Hardware registers: 24: Clock Disable State                                                                                   |
| Property | clk74_dis_st    | UChar |                 | Volatile,<br>Writable  |         |                    |         | Hardware registers: 25                                                                                                        |
| Property | ms_div_params   | UChar | 2x8             | Readable,<br>Writable  |         |                    |         | Hardware registers: 26 - 41: Feedback Multisynth Divider Parameters (doc section 3.2) - one set per PLL (NOT per MS output)   |
| Property | ms_0_5_params   | UChar | 6x8             | Readable,<br>Writable  |         |                    |         | Hardware registers: 42 - 89: Output Multisynth Parameters (doc section 4.1) - one set of 8 regs per MS output for the first 6 |
| Property | ms_6_7_params   | UChar | 2               | Readable,<br>Writable  |         |                    |         | Hardware registers: 90 - 91: Output Multisynth Parameters (doc section 4.1) - one register per MS output for the last 2       |
| Property | clk67_div       | UChar |                 | Readable,<br>Writable  |         |                    |         | Hardware registers: 92: Clock 6-7 Output divider                                                                              |
| Property | pad0            | UChar | 56              |                        | true    |                    |         | Hardware registers: 93 - 148: Padding                                                                                         |

|          |              |       |    |                       |      |  |  |                                                            |
|----------|--------------|-------|----|-----------------------|------|--|--|------------------------------------------------------------|
| Property | ss_params    | UChar | 13 | Readable,<br>Writable |      |  |  | Hardware registers: 149 - 161: Spread Spectrum Parameters  |
| Property | vcx          | UChar | 3  | Readable,<br>Writable |      |  |  | Hardware registers: 162 - 164: VCXO Parameters             |
| Property | clk_phs_offs | UChar | 6  | Readable,<br>Writable |      |  |  | Hardware registers: 165 - 170: Initial Phase Offsets       |
| Property | reserved02   | UChar | 6  |                       | true |  |  | Hardware registers: 171 - 176: Reserved                    |
| Property | pll_reset    | UChar |    | Readable,<br>Writable |      |  |  | Hardware registers: 177: PLL Reset                         |
| Property | reserved16   | UChar | 5  |                       | true |  |  | Hardware registers: 178-182: Reserved                      |
| Property | xtal_cl      | UChar |    | Readable,<br>Writable |      |  |  | Hardware registers: 183: Crystal Internal Load Capacitance |
| Property | reserved03   | UChar | 3  |                       | true |  |  | Hardware registers: 184-186: Reserved                      |
| Property | fanout_en    | UChar |    | Readable,<br>Writable |      |  |  | Hardware registers: 187: Fanout enable                     |
| Property | reserved04   | UChar | 68 |                       | true |  |  | Hardware registers: 188-255: Reserved                      |

Component Ports

Worker Interfaces

si5351.hdl

| Type             | Name   | DataWidth | Advanced       | Usage                                                                                                                                               |
|------------------|--------|-----------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| RawProp          | rprops | -         | Master=true    | Raw properties connection for slave I2C device worker                                                                                               |
| ControlInterface | -      | -         | Timeout=131072 | Control clock cycles required to complete property read/write. I2C transactions require additional clock cycles to complete than the default of 16. |

## Control Timing and Signals

### si5351.hdl

The SI5351 HDL device worker uses the clock from the Control Plane and standard Control Plane signals. There are no ports and therefore no latency or pipeline delay concerns to consider.

## Performance and Resource Utilization

### si5351.hdl

## References

- [1] SI5351 A/B/C-B I2C-PROGRAMMABLE ANY-FREQUENCY CMOS CLOCK GENERATOR + VCXO  
<https://www.silabs.com/documents/public/data-sheets/Si5351-B.pdf>