OpenCPI
CDC Fifo Tester Component Data Sheet

OpenCPI Release: v2.3.4

Revision History

Revision	Description of Change	Date
v1.6	Initial Release	02/2020

Summary - CDC Fifo Tester

Name	cdc_fifo_tester
Worker Type	Application Worker
OpenCPI Release	v2.3.4
Last Update	02/2020
Component Library	ocpi.assets.misc_comps
Workers	cdc_fifo_tester.hdl
Tested Platforms	isim, xsim, ZedBoard(PL)

Functionality

The cdc_fifo_tester serves as a testbench for the `fifo` cdc primitive. The `fifo` primitive synchronizes a mulitple bits from the source clock domain to the destination clock domain and is a FIFO where the enqueue and dequeue sides are in different clock domains. There are no restrictions with respect to clock frequencies. The output of the synchronizer is sent to worker's output port.

Worker Implementation Details

The cdc_fifo_tester worker uses a LFSR to generate data and the bits shifted out from LFSR are then used as the input to the `fifo` primitive. The data from the LFSR is enqueued as long as `fifo` is not full. The data is dequeued from the `fifo` primitive when the output port is ready for the data and the `fifo` is not empty.

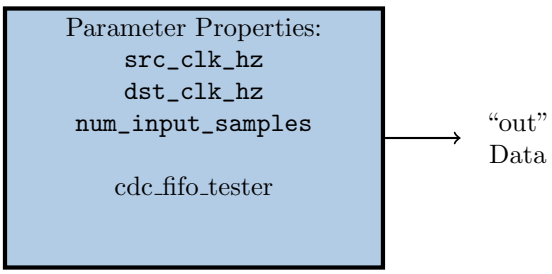
The `src_clk_hz` and `dst_clk_hz` parameter properties are used to define the source and destination domain clock frequencies.

A clock generator is used to generate the clocks for the source and destination clock domains when the source and destination clock domains are different.

Block Diagrams

Top level

Top level



Source Dependencies

cdc_fifo_tester.hdl

- assets/components/misc_comps/cdc_fifo_tester.hdl/cdc_fifo_tester.vhd
- core/hdl/primitives/cdc/fifo.vhd
- core/hdl/primitives/cdc/cdc_pkg.vhd

Component Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Description
src_clk_hz	Float	-	-	Parameter	Standard	100000000.0	Source clock frequency
dst_clk_hz	Float	-	-	Parameter	Standard	100000000.0	Destination clock frequency
num_input_samples	Uchar	-	-	Parameter	Standard	15	Number of input samples sent.

Worker Properties

cdc_fifo_tester.hdl

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Description
src_clk_hz	Float	-	-	Parameter	Standard	100000000.0	Source clock frequency
dst_clk_hz	Float	-	-	Parameter	Standard	100000000.0	Destination clock frequency
num_input_samples	Uchar	-	-	Parameter	Standard	15	Number of input samples sent.

Component Ports

Name	Producer	Protocol	Optional
out	True	(none)	False

Worker Interfaces

cdc_fifo_tester.hdl

Type	Name	Producer	Protocol	Optional	DataWidth	Clock	ClockDirection	WorkerEOF	InsertEOM
StreamInterface	out	True	(none)	False	32	-	out	True	True

Data Timing and Signals

The cdc_fifo_tester worker uses the clock from the Control Plane as input to the clock generator. The output of the clock generator is used to drive the output port clock.

Performance and Resource Utilization

Test and Verification

There are files used to validate the data the cdc_fifo_tester worker sends. The files used in the verification were created from the output of the unit test when running the unit test in simulation and contain the expected output data when there is no metastability. Since there might or might not be a perfect match of the output data to the expected output data when running the tests in hardware due to metastability or phase offset, the output data is correlated with the expected output data. If there is at least a 0.7 positive Pearson product-moment correlation coefficient, then test case is considered passing. This correlation is only used when running the unit test on hardware. If the test are run in simulation, the output data is compared with expected output data. If the they match exactly, then test case is considered passing.