OpenCPI
AD9361 DAC Sub Component Data Sheet

OpenCPI Release: v2.3.4

Summary - AD9361 DAC Sub

Name	ad9361_dac_sub
Worker Type	Device
OpenCPI Release	v2.3.4
Last Update	06/2020
Component Library	ocpi.assets.devices
Workers	ad9361_dac_sub.hdl
Tested Platforms	• Agilent Zedboard/Analog Devices FMCOMMS2 • Agilent Zedboard/Analog Devices FMCOMMS3 • x86/Xilinx ML605/Analog Devices FMCOMMS2 (FMC-LPC slot only) • x86/Xilinx ML605/Analog Devices FMCOMMS3 (FMC-LPC slot only) • Ettus E310 (Vivado only, tested via ad9361_dac_sub.test in av.bsp.e310 project)

Functionality

The AD9361 DAC Sub is a subdevice worker whose primary purpose is to time-interleave data streams for two TX channels in preparation for sending to the AD9361 IC pins (independent of which of the IC's P0/P1 buses the TX data streams are sent to). Time-interleaving occurs according to the timing diagrams specified in [2]. This worker ingests data from at most two instances of the ad9361_dac.hdl device worker, each which handles a single TX channel data stream, and time-interleaves all channels onto a single data bus that is sent out eventually (via devsignals to ad9361_data_sub.hdl[4]) to the appropriate TX data stream pins of the AD9361 IC[1].

Worker Implementation Details

ad9361_dac_sub.hdl

The ad9361_dac_sub.hdl subdevice worker handles registering and interleaving of two independent TX data streams which are sent to this worker via the `dev_data_ch0_in` and `dev_data_ch1_in` devsignal ports. Data is sent out via the `dev_data_to_pins` devsignal port which ad9361_data_sub.hdl routes to the AD9361[4]. This worker's `LVDS_p`, `HALF_DUPLEX_p`, `SINGLE_PORT_p`, and `DATA_RATE_CONFIG_p` parameter properties enforce build-time configuration for all of the possible AD9361 TX data time-interleaved modes. The currently supported modes and their limitations are shown in the following table.

Table 1: Supported DAC Sampling Rates per TX channel

Platform/Cards which allow the AD9361 Data Port/Channel Mode	AD9361 Data Port Mode	AD9361 Channel Mode	Max AD9361-Supported Sampling Rate per TX channel	Max ad9361_dac_sub.hdl-Supported Sampling Rate per TX channel
E310	CMOS Single Port Half Duplex SDR			not yet supported
E310	CMOS Single Port Half Duplex DDR			not yet supported
E310	CMOS Single Port Full Duplex SDR			not yet supported
E310	CMOS Single Port Full Duplex DDR			not yet supported
E310	CMOS Dual Port Half Duplex SDR			not yet supported
E310	CMOS Dual Port Half Duplex DDR			not yet supported
E310	CMOS Dual Port Full Duplex SDR			not yet supported
E310	CMOS Dual Port Full Duplex DDR			not yet supported
E310	CMOS Single Port Full Duplex DDR	1R1T, 2R2T Timing=0	30.72 Msps	30.72 Msps
		1R1T, 2R2T Timing=1 2R1T 1R2T	15.36 Msps	15.36 Msps
FMCOMMS2/3	LVDS (Dual Port Full Duplex DDR)	all configs	61.44 Msps	61.44 Msps[1]

[1]There are limited guarantees of data fidelity on the FMCOMMS2/3 cards for certain multichannel modes on certain platforms, although tests at room temperature have always yielded 100% fidelity.

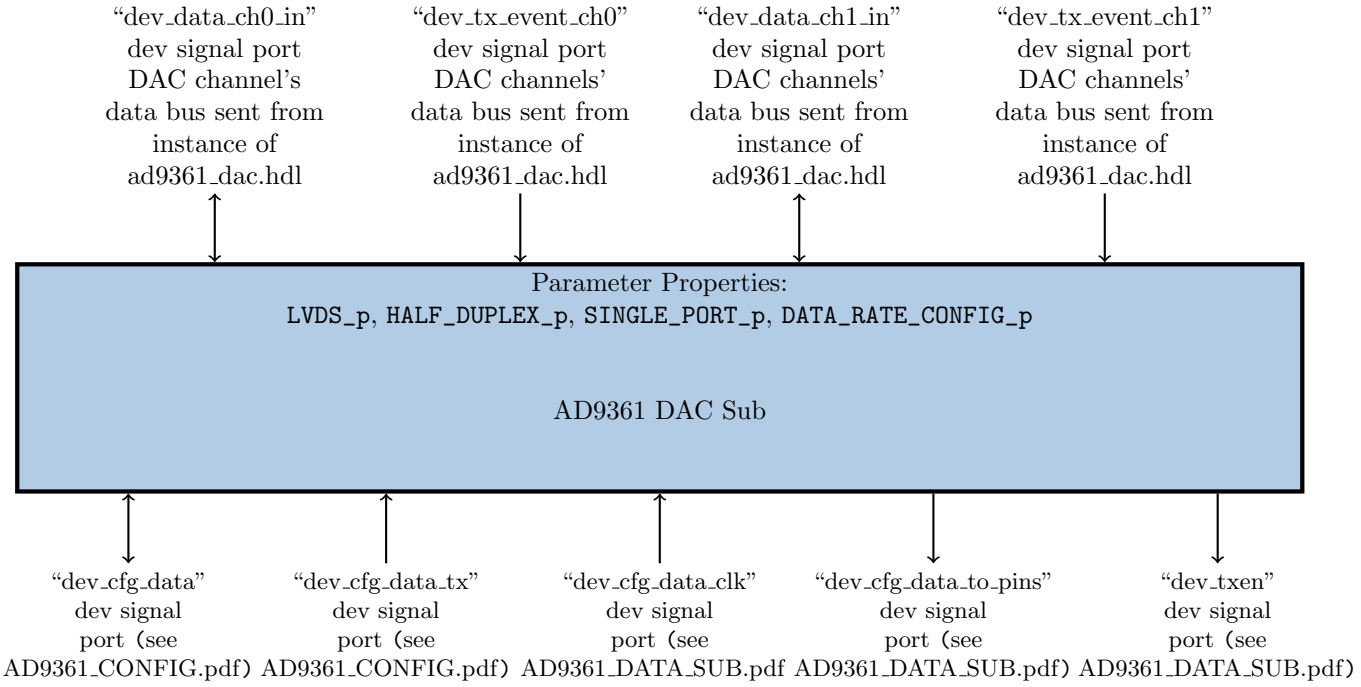
Note that "channel 0" within the context of this worker corresponds to the AD9361 T1 channel and "channel 1" corresponds to the AD9361 T2 channel in the AD9361 timing diagrams[2]. The mapping between the AD9361's T1/T2 channels and the AD9361 physical TX connector outputs is variable depending on the AD9361 register configuration. This relationship is shown in the following table. Due to the AD9361's T2 behavior[3], channel 1 should only ever be used when 2 TX channels are desired.

Table 2: Channel Connectivity (D.C. means Don't Care.)

ad9361_dac_sub.hdl devsignal channel	AD9361 timing diagram channel	AD9361 TX RF Port	AD9361 Register 0x010 Bit D5[4] (channel swap)	AD9361 Register 0x002 Bits [D7 D6][5] (channel enable)	AD9361 Register 0x004 Bit D6 (port select)
0	T1	TX1A	0	[D.C. 1]	0
0	T1	TX1B	0	[D.C. 1]	1
0	T1	TX2A	1	[1 D.C.]	0
0	T1	TX2B	1	[1 D.C.]	1
1 [3]	T2 [3]	TX2A	0	[1 1]	0
1 [3]	T2 [3]	TX2B	0	[1 1]	1
1 [3]	T2 [3]	TX1A	1	[1 1]	0
1 [3]	T2 [3]	TX1B	1	[1 1]	1

Block Diagrams

Top level



[2]For more info, see e.g. Figure 80 in [2].

[3]Data sent via T2 is only ever transmitted when the AD9361 register 0x002 Bits D7 and D6 are 1 (which corresponds to one of 1R2T or 2R2T modes).

[4]Note that AD9361 register 0x010 Bit D5 is controlled by no-OS's AD9361_InitParam struct's tx_channel_swap_enable member[2] and that the ad9361_config_proxy.rcc worker's `ad9361_init` property sets that member value[6].

[5]Note that AD9361 register 0x002 Bits [D7 D6] are controlled by no-OS's AD9361_InitParam struct's one_rx_one_tx_use_tx_num member and two_rx_two_tx_mode_enable member[2] and that the ad9361_config_proxy.rcc worker's `ad9361_init` property sets these member values[6].

Source Dependencies

ad9361_dac_sub.hdl

- assets/hdl/devices/ad9361_dac_sub.hdl/ad9361_dac_sub_cmos_single_port_fdd_ddr.vhd
- assets/hdl/devices/ad9361_dac_sub.hdl/ad9361_dac_sub.vhd
- assets/hdl/devices/ad9361_dac_sub.hdl/ad936x_tx_data_cmos_single_port_fdd_ddr.vhd
- assets/hdl/devices/ad9361_dac_sub.hdl/event_in_x2_to_txen.vhd
- assets/hdl/primitives/bsv/imports/SyncBit.v
- assets/hdl/primitives/bsv/bsv_pkg.vhd

Component Spec Attributes

Attribute	Value
NoControl	True

Component Spec Properties

Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
-	-	-	-	-	-	-	-

Worker Properties

ad9361_dac_sub.hdl

Scope	Name	Type	SequenceLength	ArrayDimensions	Accessibility	Valid Range	Default	Usage
Property	`LVDS_p`	Bool	-	-	Parameter	Standard	False	Use LVDS TX data bus interleaving scheme, otherwise use CMOS interleaving scheme. Default is CMOS.
Property	`HALF_DUPLEX_p`	Bool	-	-	Parameter	Standard	False	Use half duplex mode, otherwise use full duplex mode. Must be false when using LVDS mode.
Property	`SINGLE_PORT_p`	Bool	-	-	Parameter	Standard	False	Use single port, otherwise use both (dual) ports. Default is to use both ports. Must be false when using LVDS mode.
Property	`DATA_RATE_CONFIG_p`	Enum	-	-	Parameter	SDR, DDR	DDR	This should have a value of DDR when `LVDS_p` has a value of true. Either value is acceptable when `LVDS_p` has a value of false (i.e. CMOS mode is used).

Component Ports

Name	Producer	Protocol	Optional	Advanced	Usage
-	-	-	-	-	-

Worker Interfaces

ad9361_dac_sub.hdl

Type	Name	Count	Optional	Master	Signal	Direction	Width	Description
DevSignal	dev_cfg_data	1	False	True	config_is_two_r	Input	1	Some data port configurations (such as LVDS) require the TX bus to use 2R2T timing if either 2 TX or 2 RX channels are used. For example, if using LVDS and this has a value of 1, 2R2T timing will be forced.
					ch0_handler_is_present	Output	1	Value is 1 if the dev_data_ch0 dev signal is connected to a worker (that "handles" the data) and 0 otherwise. This is expected to be hardcoded at buildtime.
					ch1_handler_is_present	Output	1	Value is 1 if the dev_data_ch1 dev signal is connected to a worker (that "handles" the data) and 0 otherwise. This is expected to be hardcoded at buildtime.
					data_bus_index_direction	Output	1	Value is 1 if the bus indexing of the P0_D/P1_D signals from dev_data_from_pins was reversed before processing. This is expected to be hardcoded at buildtime.
					data_clk_is_inverted	Output	1	Value is 1 if the clock in via dev_data_clk was inverted inside this worker before used as an active-edge rising clock. This is expected to be hardcoded at buildtime.
					islvds	Output	1	Value is 1 if `LVDS_p` has a value of true and 0 if `LVDS_p` has a value of false. Because `LVDS_p` is a parameter property, this is hardcoded at buildtime. The purpose of this devsignal is to feed this worker's buildtime-specified LVDS/CMOS mode through ad9361_config.hdl to ad9361_config_proxy.rcc so No-OS knows which LVDS/CMOS mode to use when initializing the AD9361 IC.
					isdualport	Output	1	Value is 1 if `SINGLE_PORT_p` has a value of false and 0 if `SINGLE_PORT_p` has a value of true. Because `SINGLE_PORT_p` is a parameter property, this is hardcoded at buildtime. The purpose of this devsignal is to feed this worker's buildtime-specified single/dual port mode through ad9361_config.hdl to ad9361_config_proxy.rcc so No-OS knows which single/dual port mode to use when initializing the AD9361 IC.
					isfullduplex	Output	1	Value is 1 if `HALF_DUPLEX_p` has a value of false and 0 if `HALF_DUPLEX_p` has a value of true. Because `HALF_DUPLEX_p` is a parameter property, this is hardcoded at buildtime. The purpose of this devsignal is to feed this worker's buildtime-specified half/full duplex mode through ad9361_config.hdl to ad9361_config_proxy.rcc so No-OS knows which half/full duplex mode to use when initializing the AD9361 IC.
					isDDR	Output	1	Value is 1 if `DATA_RATE_CONFIG_p` has a value of DDR and 0 if `DATA_RATE_CONFIG_p` has a value of SDR. Because `DATA_RATE_CONFIG_p` is a parameter property, this is hardcoded at buildtime. The purpose of this devsignal is to feed this worker's buildtime-specified SDR/DDR mode through ad9361_config.hdl to ad9361_config_proxy.rcc so No-OS knows which half/full duplex mode to use when initializing the AD9361 IC.
					present	Output	1	Used to communicate to ad9361_config.hdl that it should validate the islvds, isdualport, isfullduplex, and isddr signals against similar signals in the ad9361_adc_sub.hdl and ad9361_data_sub.hdl workers if they are present in the bitstream. This is expected to be hardcoded at buildtime.

DevSignal	dev_cfg_data_tx	1	False	True	config_is_two_t	Input	1	Some data port configurations (such as LVDS) require the TX bus to use 2R2T timing if either 2 TX or 2 RX channels are used. For example, if using LVDS and this has a value of 1, 2R2T timing will be forced.
					force_two_r_two_t_timing	Input	1	Expected to match value of AD9361 register 0x010 bit D2[3].
DevSignal	dev_data_clk	1	False	True	DATA_CLK_P	Input	1	Buffered version of AD9361 DATA_CLK_P pin.
DevSignal	dev_data_to_pins	1	False	True	data	Output	24	Data bus containing configuration-specific AD9361 pins corresponding to the TX data path: * CMOS single port half duplex: [12'b0 P0_D[11:0]], * CMOS single port full duplex: [18'b0 P0_D[11:6]], * CMOS dual port half duplex: [P0_D[11:0] P1_D[11:0]], * CMOS dual port full duplex: [12'b0 P1_D[11:0]], * LVDS: [18'b0 TX_D[5:0]], or, if ports are swapped: * CMOS single port half duplex: [12'b0 P1_D[11:0]], * CMOS single port full duplex: [18'b0 P1_D[11:6]], * CMOS dual port half duplex: [P1_D[11:0] P0_D[11:0]], * CMOS dual port full duplex: [12'b0 P0_D[11:0]], * LVDS: (unsupported with port swap). For more info see [4].
					tx_frame	Output	1	Signal which will drive the output buffer which drives the AD9361 TX_FRAME_P pin.
					fb_clk	Output	1	Signal which will drive the output buffer which will drive the AD9361 FB_CLK_P pin.
DevSignal	dev_txen	1	False	True	txen	Output	1	-
DevSignal	dev_data_ch0_in	1	False	False	present	Output	1	Value is 1 if a worker is connected to this devsignal port.
					dac_clk	Input	1	Clock for dac_ready, dac_take, dac_data_I, and dac_data_Q.
					dac_ready	Output	1	Indicates that the dac_data_I and dac_data_Q are valid/ready to be latched on the next rising edge of adc_clk.
					dac_take	Input	1	Indicates that dac_data_I and dac_data_Q were latched on the previous rising edge of dac_clk. If in the previous clock cycle dac_ready was 1, the values of dac_data_I and dac_data_Q should not be allowed to update with a new sample until dac_take is 1.
					dac_data_I	Output	12	Signed Q0.11 I value of DAC sample corresponding to RX channel 0.
					dac_data_Q	Output	12	Signed Q0.11 Q value of DAC sample corresponding to RX channel 0.
DevSignal	dev_data_ch1_in	1	True	False	present	Output	1	Value is 1 if a worker is connected to this devsignal port.
					dac_clk	Input	1	Clock for dac_ready, dac_take, dac_data_I, and dac_data_Q.
					dac_ready	Output	1	Indicates that the dac_data_I and dac_data_Q are valid/ready to be latched on the next rising edge of adc_clk.
					dac_take	Input	1	Indicates that dac_data_I and dac_data_Q were latched on the previous rising edge of dac_clk. If in the previous clock cycle dac_ready was 1, the values of dac_data_I and dac_data_Q should not be allowed to update with a new sample until dac_take is 1.
					dac_data_I	Output	12	Signed Q0.11 I value of DAC sample corresponding to RX channel 1.
					dac_data_Q	Output	12	Signed Q0.11 Q value of DAC sample corresponding to RX channel 1.
DevSignal	dev_tx_event_ch0	1	False	False	txon_pulse	Output	1	-
					txoff_pulse	Output	1	-
					event_in_connected	Output	1	-
					is_operating	Output	1	-

DevSignal	dev_tx_event_ch1	1	True	False	txon_pulse	Output	1	-
					txoff_pulse	Output	1	-
					event_in_connected	Output	1	-
					is_operating	Output	1	-

Subdevice Connections

Supports Worker	Supports Worker Port	ad9361_dac_sub.hdl Port	ad9361_dac_sub.hdl Port Index
ad9361_dac	dev_dac	dev_data_ch0_in	0
ad9361_dac	dev_dac	dev_data_ch1_in	0

Control Timing and Signals

The AD9361 DAC Sub subdevice worker contains four clock domains: control plane, FB_CLK_P, "dac_clk" and "dacd2_clk".

Control Plane Clock Domain

The `data_cfg_tx` signals enter this worker in the control plane clock domain. Inside this worker, they are combined combinatorially into a single signal which is subsequently synchronized to the dacd2_clk domain. The dacd2_clk domain signal is then used to handle time-interleaving of multiple channel's data.

DATA_CLK_P/FB_CLK_P Clock Domain

The AD9361 DATA_CLK_P clock enters this worker via the `dev_data_clk` devsignal. DATA_CLK_P clock is forwarded to the `FB_CLK_P` device signal as well as used to generate dac_clk.

"dac_clk" Clock Domain

The "dac_clk" clock is an inverted version of DATA_CLK_P. Note that data transitions for the TX data sent out via the `dev_data_to_pins` devsignal port are falling-edge aligned with `FB_CLK_P` since the falling edge is what the AD9361 datasheets specifies its setup/hold requirements against[2]. The dac_clk domain allows for logic within this worker to be falling edge aligned with `FB_CLK_P`.

"dacd2_clk" Clock Domain

The "dacd2_clk" clock is a divided by 2 version of "dac_clk". TX data for channel 0 and channel 1 enter this worker in the dacd2_clk domain from the `dev_data_ch0_in` and `dev_data_ch1_in` devsignal ports, respectively. The dacd2_clk clock was a necessary replacement for some of the dac_clk logic in order to alleviate timing violations in the dac_clk domain for the zed_ise platform. Note that because dacd2_clk is a divided version of dac_clk, synchronization logic between the two is not necessary and not included.

Data latency

- **LVDS mode and CMOS Single Port Full Duplex**
  Latency for these modes is given as the number of clock cycles from a given channel's data becoming ready on the dac_data_I and dac_data_Q devsignals to the starting edge of the high 6-bit I word on the AD9361 data bus output. Note that, for multichannel modes, latency can be two possible values depending on the current state of the 2-state channel serialization state machine when dac_data_I/dac_data_Q becomes ready. The latency for the various LVDS and CMOS Single Port Full Duplex configurations are as follows:
  - 1R1T
    channel 0 data latency = 3 FB_CLK_P cycles (2 are pipeline delay which are arguably unnecessary and 1 is a 12-bit word to 6-bit word serialization register)
  - 2R1T/1R2T/2R2T
    channel 0 data latency = 3 or 5 FB_CLK_P cycles (2 are pipeline delay which are arguably unnecessary, 2 are possible channel serialization register delay, and 1 is a 12-bit word to 6-bit word serialization register)
    channel 1 data latency = 3 or 5 FB_CLK_P cycles (2 are pipeline delay which are arguably unnecessary, 2 are possible channel serialization register delay, and 1 is a 12-bit word to 6-bit word serialization register)

Multichannel Phase Coherency

Note that the two channel data made available via dev_data_ch0_in and dev_data_ch1_in are only ever considered to be phase coherent if coherency is guaranteed by the worker(s) that dev_data_ch0_in and dev_data_ch1_in are connected to. For example, multiple instances of ad9361_dac.hdl would not guarantee phase coherence because their datastreams would be independent. However, if a single device worker was created which interfaced with both dev_data_ch0_in and dev_data_ch1_in, phase coherency could be guaranteed by updating the values for the two channels in an every-other-clock fashion.

Worker Configuration Parameters

ad9361_dac_sub.hdl

Performance and Resource Utilization

ad9361_dac_sub.hdl

Fmax refers to the maximum allowable clock rate for any registered signal paths within a given clock domain for an FPGA design. Fmax in the table below is specific only to this worker and represents the maximum possible Fmax for any OpenCPI bitstream built with this worker included. Note that the Fmax value for a given clock domain for the final bitstream is often worse than the Fmax specific to this worker, even if this worker is the only one included in the bitstream.

In the tables below, dev_data_clk is the worker source code name for the signal which is ultimately driven by, and has the same clock rate of, the AD9361 DATA_CLK pin pair.

Table 4: Resource Utilization Table for worker: ad9361_dac_sub

Configuration	OCPI Target	Tool	Version	Device	Registers (Typ)	LUTs (Typ)	Fmax (MHz) (Typ)		Memory/Special Functions
							control plane clock	dev_data_clk clock	
0	zynq	Vivado	2017.1	xc7z020clg484-1	94	89	477 [1]	267 [1]	ODDR: 7 BUFR: 1
0	virtex6	ISE	14.7	6vlx240tff1156-1	101	113	689.655	632.511	ODDR: 7 BUFR: 1
1	zynq	Vivado	2017.1	xc7z020clg484-1	24	36	477 [1]	297 [1]	ODDR: 7
1	virtex6	ISE	14.7	6vlx240tff1156-1	29	44	689.655	496.416	ODDR: 7

Test and Verification

The test outlined in [5] includes validation of this worker's functionality (for LVDS mode and CMOS Single Port Full Duplex DDR mode only).

[1] These measurements were the result of a Vivado timing analysis which was different from the Vivado analysis performed by default for OpenCPI worker builds. For more info see Appendix 1

[2] Quartus does not perform timing analysis at the OpenCPI worker build (i.e. synthesis) stage.

References

[1] AD9361 Datasheet and Product Info
`https://www.analog.com/en/products/ad9361.html`

[2] AD9361 Reference Manual UG-570
AD9361_Reference_Manual_UG-570.pdf

[3] AD9361 Register Map Reference Manual UG-671
AD9361_Register_Map_Reference_Manual_UG-671.pdf

[4] AD9361 Data Sub Component Data Sheet
`http://opencpi.gitlab.io/releases/v2.3.4/docs/assets/AD9361_Data_Sub.pdf`

[5] AD9361 DAC Component Data Sheet
`http://opencpi.gitlab.io/releases/v2.3.4/docs/assets/AD9361_DAC.pdf`

[6] AD9361 Config Proxy Component Data Sheet
`http://opencpi.gitlab.io/releases/v2.3.4/docs/assets/AD9361_Config_Proxy.pdf`

1 Appendix - Vivado Timing Analysis

The Vivado timing report that OpenCPI runs for HDL worker builds will erroneously report a max delay for a clocking path which should be ignored. Custom Vivado tcl commands have to be run in order to extract pertinent information from Vivado timing analysis. After building the worker, the following commands were run from the assets project directory (after the Vivado settings64.sh was sourced):

```
cd hdl/devices/
vivado -mode tcl
```

Then the following commands were run inside the Vivado tcl terminal:

```
open_project ad9361_dac_sub.hdl/target-zynq/ad9361_dac_sub_rv.xpr
synth_design -part xc7z020clg484-1 -top ad9361_dac_sub_rv -mode out_of_context
create_clock -name clk1 -period 0.001 [get_nets wci_Clk]
create_clock -name clk2 -period 0.001 [get_nets dev_data_clk*]
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]
report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
report_timing -delay_type min_max -sort_by slack -input_pins -group clk2
close_project
open_project ad9361_dac_sub.hdl/target-1-zynq/ad9361_dac_sub_rv.xpr
synth_design -part xc7z020clg484-1 -top ad9361_dac_sub_rv_c1 -mode out_of_context
create_clock -name clk1 -period 0.001 [get_nets wci_Clk]
create_clock -name clk2 -period 0.001 [get_nets dev_data_clk*]
set_clock_groups -asynchronous -group [get_clocks clk1] -group [get_clocks clk2]
report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
report_timing -delay_type min_max -sort_by slack -input_pins -group clk2
close_project
```

The following commands are run to get the slack for all clocks:

```
report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
```

The Fmax for each clock for this worker is computed as the inverse of [(maximum slack magnitude with the vivado-configured clock rate of 1 ps) plus (2 times the assumed 1 ps control plane clock period)], e.g. 1/[(5.372 ns) + (0.002 ns)] = 186.08 MHz = Fmax.

An example output for is as follows:

```
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
WARNING: [Timing 38-242] The property HD.CLK_SRC of clock port "ctl_in[Clk]" is not set. In out-of-context mode, this prevents timing estimation for clock \
      delay/skew
Resolution: Set the HD.CLK_SRC property of the out-of-context port to the location of the clock buffer instance in the top-level design
WARNING: [Timing 38-242] The property HD.CLK_SRC of clock port "dev_dac_in[dac_clk]" is not set. In out-of-context mode, this prevents timing estimation for \
      clock delay/skew
Resolution: Set the HD.CLK_SRC property of the out-of-context port to the location of the clock buffer instance in the top-level design
INFO: [Timing 38-78] ReportTimingParams: -max_paths 1 -nworst 1 -delay_type min_max -sort_by slack.
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------------------------------------------------------------------------------------------------
| Tool Version : Vivado v.2017.1 (lin64) Build 1846317 Fri Apr 14 18:54:47 MDT 2017
| Date         : Wed Oct 3 16:41:06 2018
| Host         : <removed> running 64-bit CentOS Linux release 7.5.1804 (Core)
| Command      : report_timing -delay_type min_max -sort_by slack -input_pins -group clk1
| Design       : ad9361_dac_rv
| Device       : 7z020-clg484
```

```
| Speed File  : -1 PRODUCTION 1.11 2014-09-11
------------------------------------------------------------------------------------------------

Timing Report

Slack (VIOLATED) :      -5.372ns (required time - arrival time)
 Source:                IN_port/fifo/data0_reg_reg[13]/C
                          (rising edge-triggered cell FDRE clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
 Destination:           worker/fifo/fifo/fifoMem_reg/DIADI[9]
                          (rising edge-triggered cell RAMB18E1 clocked by clk1 {rise@0.000ns fall@0.001ns period=0.001ns})
 Path Group:            clk1
 Path Type:             Setup (Max at Slow Process Corner)
 Requirement:           0.002ns (clk1 rise@0.002ns - clk1 rise@0.000ns)
 Data Path Delay:       4.374ns (logic 1.904ns (43.533%) route 2.470ns (56.467%))
 Logic Levels:          5  (CARRY4=3 LUT4=1 LUT5=1)
 Clock Path Skew:       -0.049ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD): 0.924ns = ( 0.926 - 0.002 )
   Source Clock Delay    (SCD):   0.973ns
   Clock Pessimism Removal (CPR): 0.000ns
 Clock Uncertainty:    0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter  (TSJ):   0.071ns
   Total Input Jitter   (TIJ):   0.000ns
   Discrete Jitter       (DJ):   0.000ns
   Phase Error           (PE):   0.000ns

   Location           Delay type             Incr(ns) Path(ns)   Netlist Resource(s)
 ------------------------------------------------------------------- -------------------
                     (clock clk1 rise edge)    0.000    0.000 r
                                               0.000    0.000 r ctl_in[Clk] (IN)
                     net (fo=198, unset)       0.973    0.973   IN_port/fifo/ctl_in[Clk]
                     FDRE                                    r  IN_port/fifo/data0_reg_reg[13]/C
 ------------------------------------------------------------------- -------------------
                     FDRE (Prop_fdre_C_Q)      0.518    1.491 r IN_port/fifo/data0_reg_reg[13]/Q
                     net (fo=3, unplaced)      0.759    2.250   IN_port/fifo/IN_data[5]
                                                         r  IN_port/fifo/fifoMem_reg_i_36/I1
                     LUT4 (Prop_lut4_I1_O)     0.295    2.545 r IN_port/fifo/fifoMem_reg_i_36/O
                     net (fo=1, unplaced)      0.902    3.447   IN_port/fifo/fifoMem_reg_i_36_n_0
                                                         r  IN_port/fifo/fifoMem_reg_i_24/I1
                     LUT5 (Prop_lut5_I1_O)     0.124    3.571 r IN_port/fifo/fifoMem_reg_i_24/O
                     net (fo=1, unplaced)      0.000    3.571   IN_port/fifo/fifoMem_reg_i_24_n_0
                                                         r  IN_port/fifo/fifoMem_reg_i_5/S[0]
                     CARRY4 (Prop_carry4_S[0]_CO[3])
                                               0.513    4.084 r IN_port/fifo/fifoMem_reg_i_5/CO[3]
                     net (fo=1, unplaced)      0.009    4.093   IN_port/fifo/fifoMem_reg_i_5_n_0
                                                         r  IN_port/fifo/fifoMem_reg_i_4/CI
                     CARRY4 (Prop_carry4_CI_CO[3])
                                               0.117    4.210 r IN_port/fifo/fifoMem_reg_i_4/CO[3]
                     net (fo=1, unplaced)      0.000    4.210   IN_port/fifo/fifoMem_reg_i_4_n_0
                                                         r  IN_port/fifo/fifoMem_reg_i_3/CI
                     CARRY4 (Prop_carry4_CI_O[1])
                                               0.337    4.547 r IN_port/fifo/fifoMem_reg_i_3/O[1]
                     net (fo=1, unplaced)      0.800    5.347   worker/fifo/fifo/sD_IN[9]
                     RAMB18E1                                r  worker/fifo/fifo/fifoMem_reg/DIADI[9]
 ------------------------------------------------------------------- -------------------

                     (clock clk1 rise edge)    0.002    0.002 r
                                               0.000    0.002 r ctl_in[Clk] (IN)
```

```
                    net (fo=198, unset)       0.924    0.926   worker/fifo/fifo/ctl_in[Clk]
                    RAMB18E1                                r  worker/fifo/fifo/fifoMem_reg/CLKBWRCLK
                    clock pessimism           0.000    0.926
                    clock uncertainty        -0.035    0.891
                    RAMB18E1 (Setup_ramb18e1_CLKBWRCLK_DIADI[9])
                                             -0.916   -0.025   worker/fifo/fifo/fifoMem_reg
  -------------------------------------------------------------------
                    required time                     -0.025
                    arrival time                      -5.347
  -------------------------------------------------------------------
                    slack                             -5.372




report_timing: Time (s): cpu = 00:00:08 ; elapsed = 00:00:09 . Memory (MB): peak = 2095.184 ; gain = 497.547 ; free physical = 7704 ; free virtual = 54670
```

The following command is run to get dev_dac.dac_clk timing:

```
report_timing -delay_type min_max -sort_by slack -input_pins -group clk2
```

The expected output of the command is as follows:

```
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
INFO: [Timing 38-78] ReportTimingParams: -max_paths 1 -nworst 1 -delay_type min_max -sort_by slack.
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------------------------------------------------------------------------------------------------
| Tool Version : Vivado v.2017.1 (lin64) Build 1846317 Fri Apr 14 18:54:47 MDT 2017
| Date        : Thu Oct 4 10:56:37 2018
| Host        : <removed> running 64-bit CentOS Linux release 7.5.1804 (Core)
| Command     : report_timing -delay_type min_max -sort_by slack -input_pins -group clk2
| Design      : ad9361_dac_rv
| Device      : 7z020-clg484
| Speed File  : -1  PRODUCTION 1.11 2014-09-11
------------------------------------------------------------------------------------------------


Timing Report

Slack (VIOLATED) :     -4.306ns (required time - arrival time)
  Source:              worker/fifo/fifo/dEnqPtr_reg[0]/C
                         (rising edge-triggered cell FDCE clocked by clk2 {rise@0.000ns fall@0.001ns period=0.001ns})
  Destination:         worker/fifo/fifo/fifoMem_reg/ENARDEN
                         (rising edge-triggered cell RAMB18E1 clocked by clk2 {rise@0.000ns fall@0.001ns period=0.001ns})
  Path Group:          clk2
  Path Type:           Setup (Max at Slow Process Corner)
  Requirement:         0.002ns (clk2 rise@0.002ns - clk2 rise@0.000ns)
  Data Path Delay:     3.781ns (logic 1.061ns (28.063%) route 2.720ns (71.937%))
  Logic Levels:        3  (LUT2=1 LUT6=2)
  Clock Path Skew:     -0.049ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD): 0.924ns = ( 0.926 - 0.002 )
    Source Clock Delay    (SCD):   0.973ns
    Clock Pessimism Removal (CPR): 0.000ns
  Clock Uncertainty:   0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter   (TSJ):   0.071ns
    Total Input Jitter    (TIJ):   0.000ns
    Discrete Jitter        (DJ):   0.000ns
```

```
  Phase Error           (PE):   0.000ns

  Location           Delay type             Incr(ns) Path(ns)   Netlist Resource(s)
-------------------------------------------------------------------- -------------------
                     (clock clk2 rise edge)    0.000    0.000 r
                                               0.000    0.000 r dev_dac_in[dac_clk] (IN)
                     net (fo=35, unset)        0.973    0.973   worker/fifo/fifo/dev_dac_in[dac_clk]
                     FDCE                                   r  worker/fifo/fifo/dEnqPtr_reg[0]/C
-------------------------------------------------------------------- -------------------
                     FDCE (Prop_fdce_C_Q)      0.518    1.491 r worker/fifo/fifo/dEnqPtr_reg[0]/Q
                     net (fo=1, unplaced)      0.965    2.456   worker/fifo/fifo/dEnqPtr[0]
                                                       r  worker/fifo/fifo/dGDeqPtr_rep[0]_i_3/I0
                     LUT6 (Prop_lut6_I0_O)     0.295    2.751 r worker/fifo/fifo/dGDeqPtr_rep[0]_i_3/O
                     net (fo=1, unplaced)      0.449    3.200   worker/fifo/fifo/dGDeqPtr_rep[0]_i_3_n_0
                                                       r  worker/fifo/fifo/dGDeqPtr_rep[0]_i_1/I1
                     LUT6 (Prop_lut6_I1_O)     0.124    3.324 r worker/fifo/fifo/dGDeqPtr_rep[0]_i_1/O
                     net (fo=18, unplaced)     0.506    3.830   worker/fifo/fifo/dGDeqPtr0
                                                       r  worker/fifo/fifo/fifoMem_reg_i_1/I0
                     LUT2 (Prop_lut2_I0_O)     0.124    3.954 r worker/fifo/fifo/fifoMem_reg_i_1/O
                     net (fo=1, unplaced)      0.800    4.754   worker/fifo/fifo/fifoMem_reg_i_1_n_0
                     RAMB18E1                                 r  worker/fifo/fifo/fifoMem_reg/ENARDEN
-------------------------------------------------------------------- -------------------

                     (clock clk2 rise edge)    0.002    0.002 r
                                               0.000    0.002 r dev_dac_in[dac_clk] (IN)
                     net (fo=35, unset)        0.924    0.926   worker/fifo/fifo/dev_dac_in[dac_clk]
                     RAMB18E1                                 r  worker/fifo/fifo/fifoMem_reg/CLKARDCLK
                     clock pessimism           0.000    0.926
                     clock uncertainty        -0.035    0.891
                     RAMB18E1 (Setup_ramb18e1_CLKARDCLK_ENARDEN)
                                              -0.443    0.448   worker/fifo/fifo/fifoMem_reg
-------------------------------------------------------------------
                     required time                      0.448
                     arrival time                      -4.754
-------------------------------------------------------------------
                     slack                             -4.306
```